SiliconGraphics
Computer Systems
CRAY RESEARCH

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Contenido del curso

La arquitectura Origin 2000

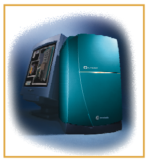
SiliconGraphics Computer Systems

CRAY RESEARCH

Gama de productos Silicon Graphics/CRAY

O^2

1 CPU
Arquitectura UMA
(Unified Memory Architecture)



Octane

1–2 CPUs
Arquitectura S2MP
(Scalable Shared–memory MultiProcessor)

Onyx2

1–16 CPUs
Arquitectura S2MP

Origin200

1–4 CPUs
1–2 torres
Arquitectura S2MP

Origin2000 Deskside

1–4 CPUs
Arquitectura S2MP

Origin2000 Rack or Multirack

1–64 CPUs
1–4 racks
Arquitectura S2MP

CRAY Origin2000

65–128 CPUs
5–8 racks
Arquitectura S2MP

CRAY J90

1–16 CPUs
Arquitectura Vectorial

CRAY T90

1–32 CPUs
Arquitectura Vectorial

CRAY T3E

16–2048 CPUs
Arquitectura MPP

Características de la CPU

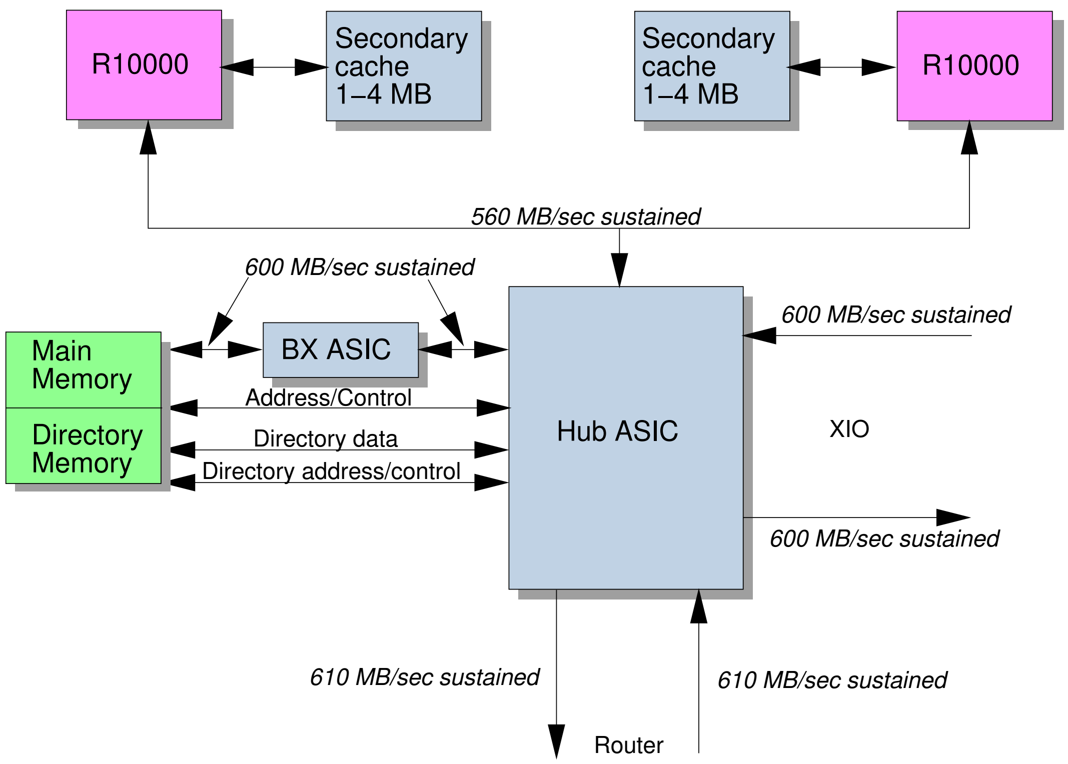
R10000 64 bit RISC MIPS

- MIPS IV Instruction Set Architecture – SuperScalar
- Out of order instruction execution
- 2 Integer Arithmetic Logical Units (ALU), load/store, floating add, floating multiply
- 32 hardware performance counters (_hwc's)
- 32Kbyte instruction and data primary cache on chip cache line size is 32B or 64Bytes
- 180MHz have 1Mbyte secondary caches

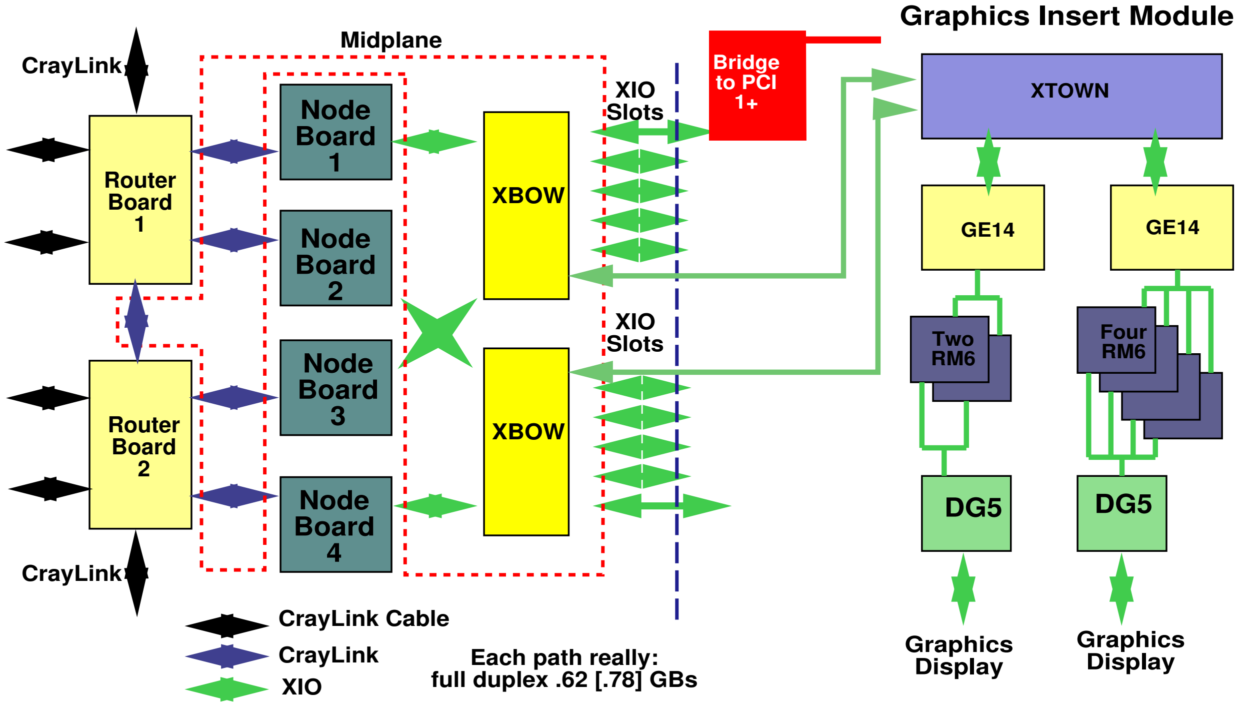
  195MHz have 4Mbyte secondary caches

  cache line size is 128Bytes

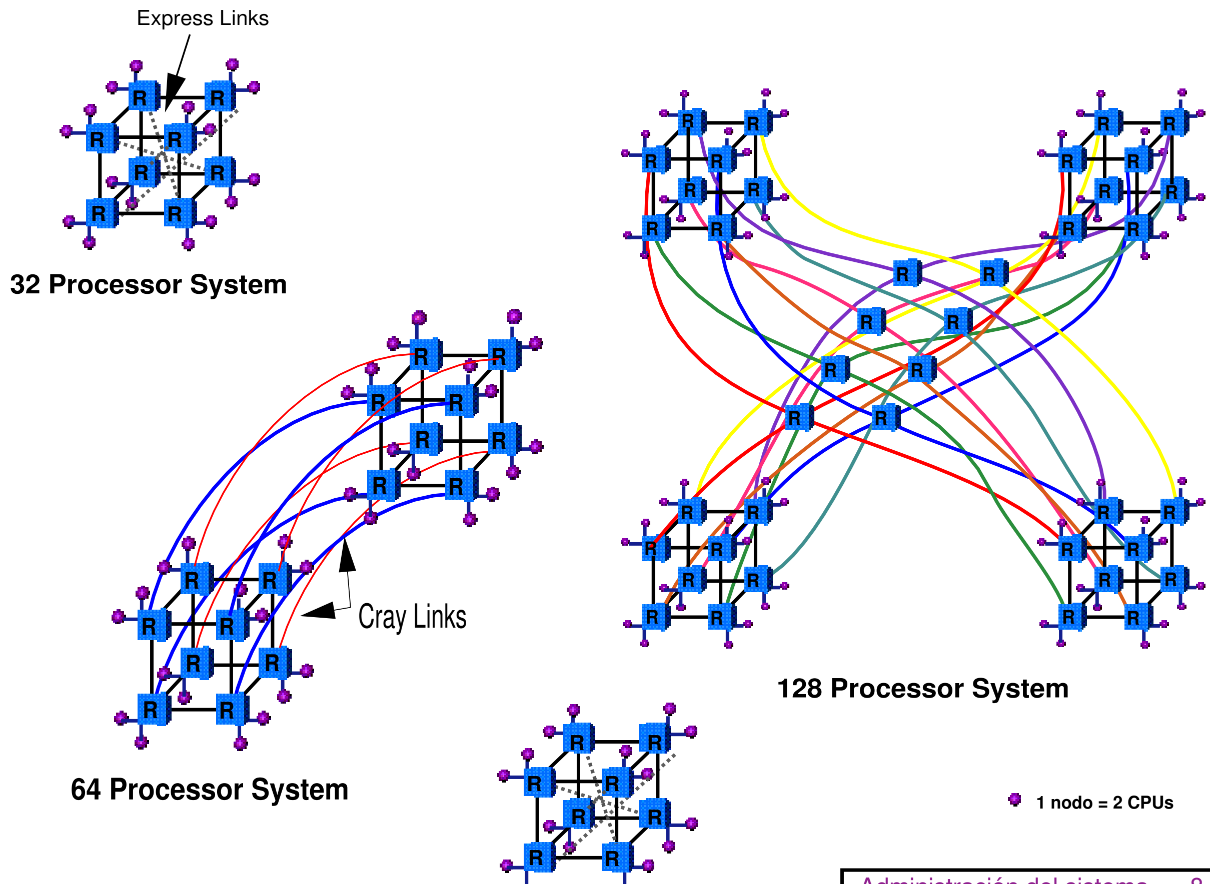
Arquitectura de 1 nodo (2 CPUs)



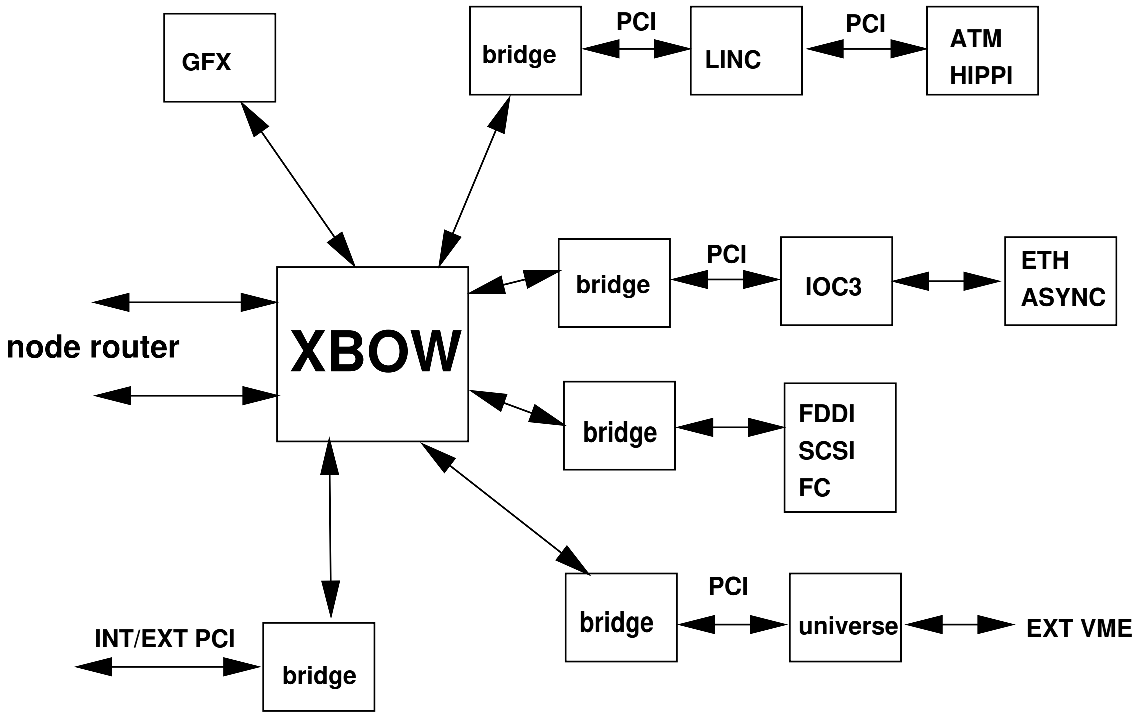
Arquitectura de 1 módulo (4 nodos, 8 cpus) con hardware gráfico (Onyx)



Origin2000 Internode Topology



I/O Architecture



Latencia local vs Latencia remota

El tiempo de acceso a memoria depende de la posición de ésta respecto a la CPU en la que está corriendo el proceso:

- La Memoria en el propio nodo se accede más rápidamente
- La Memoria en otro nodo del mismo módulo pasa por un router
- La Memoria en otros módulos pasa por sucesivos routers

Location	Latency (in cycles; 32 cpus)
Registers	0
Primary cache	1
Secondary cache	10
Home memory	61
Remote cache – 1 router away	117
Remote cache – 2 routers	137
Remote cache – 3 routers	157