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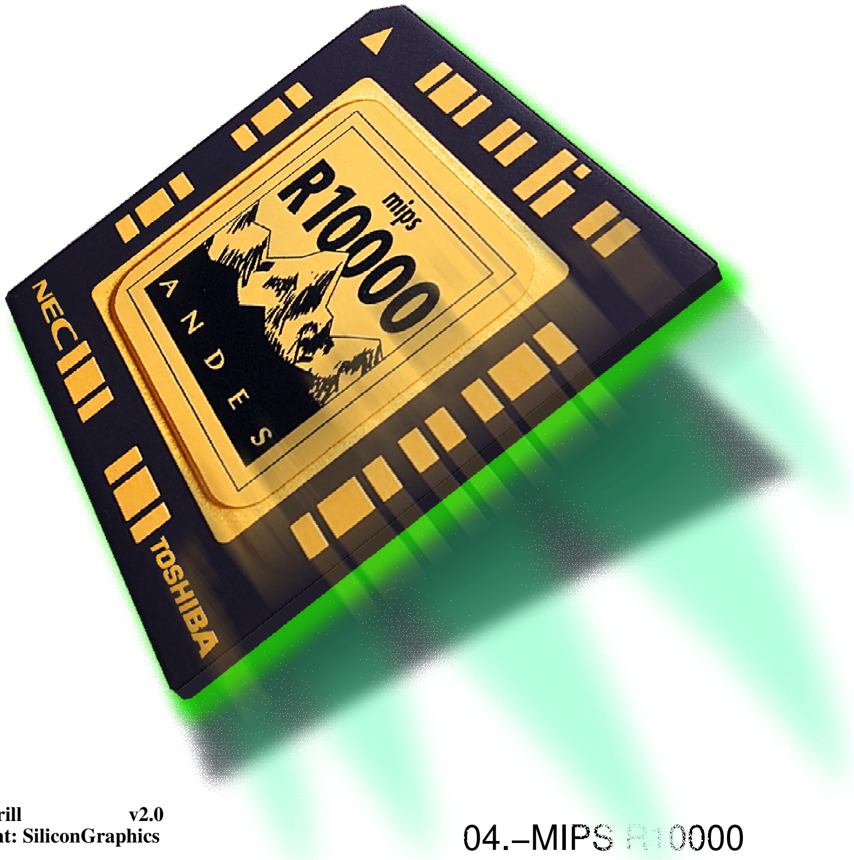
MIPS R10000™



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- MIPS: una arquitectura abierta
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MIPS: una arquitectura abierta

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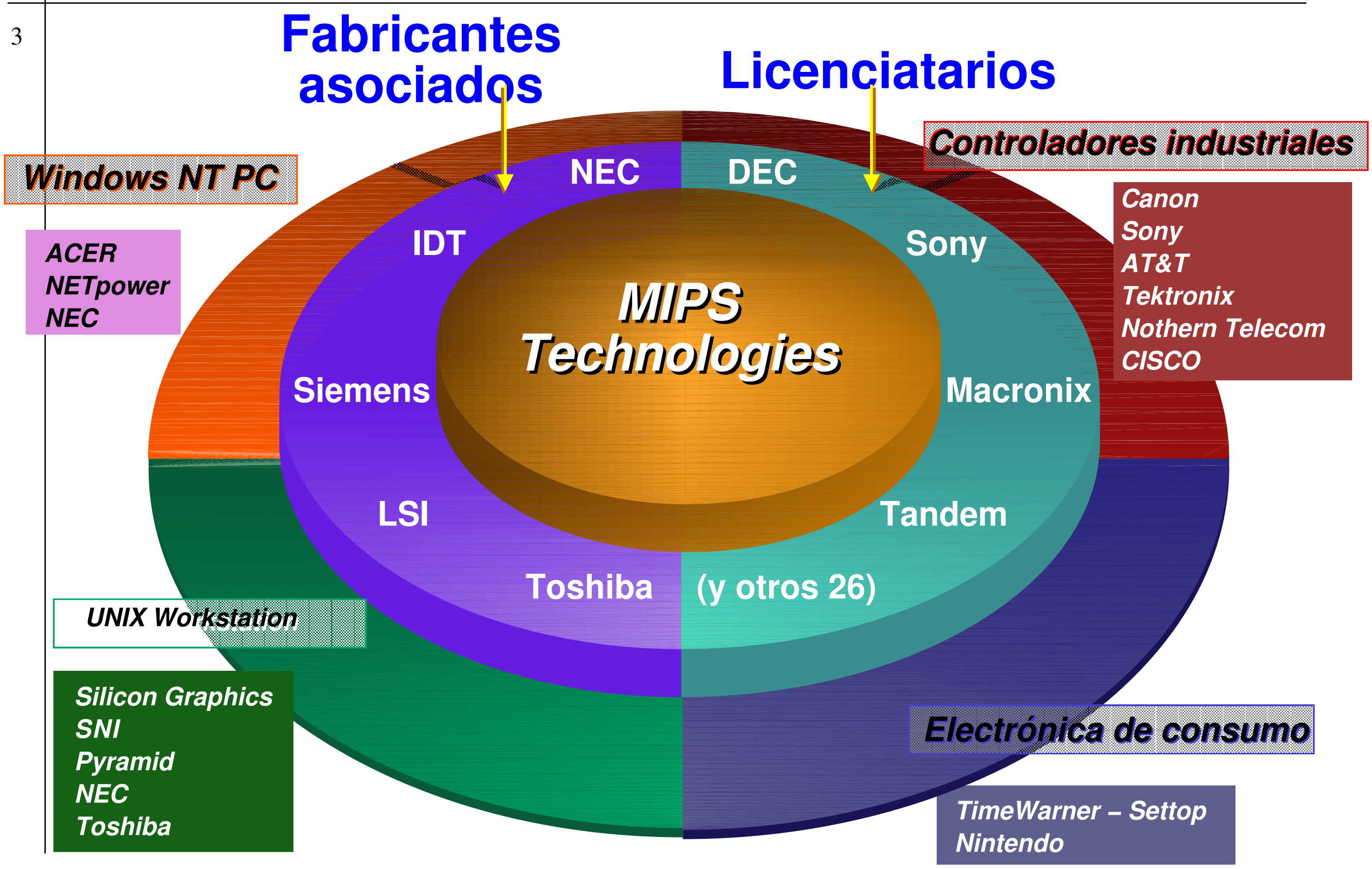

MIPS: una arquitectura abierta

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- *Empezó a diseñar chips RISC en 1.986*
- *Empezó a diseñar mProc para SMP en 1.987*
- *En 1.992 fué adquirida por SGI (100% SGI)*
- *Hoy en dia es una División dentro de SGI*
- *desde el R4000 (1.990) todos los chips son de 64 bits*
- *diseñan chips, compiladores y herramientas*

El diseño de chips

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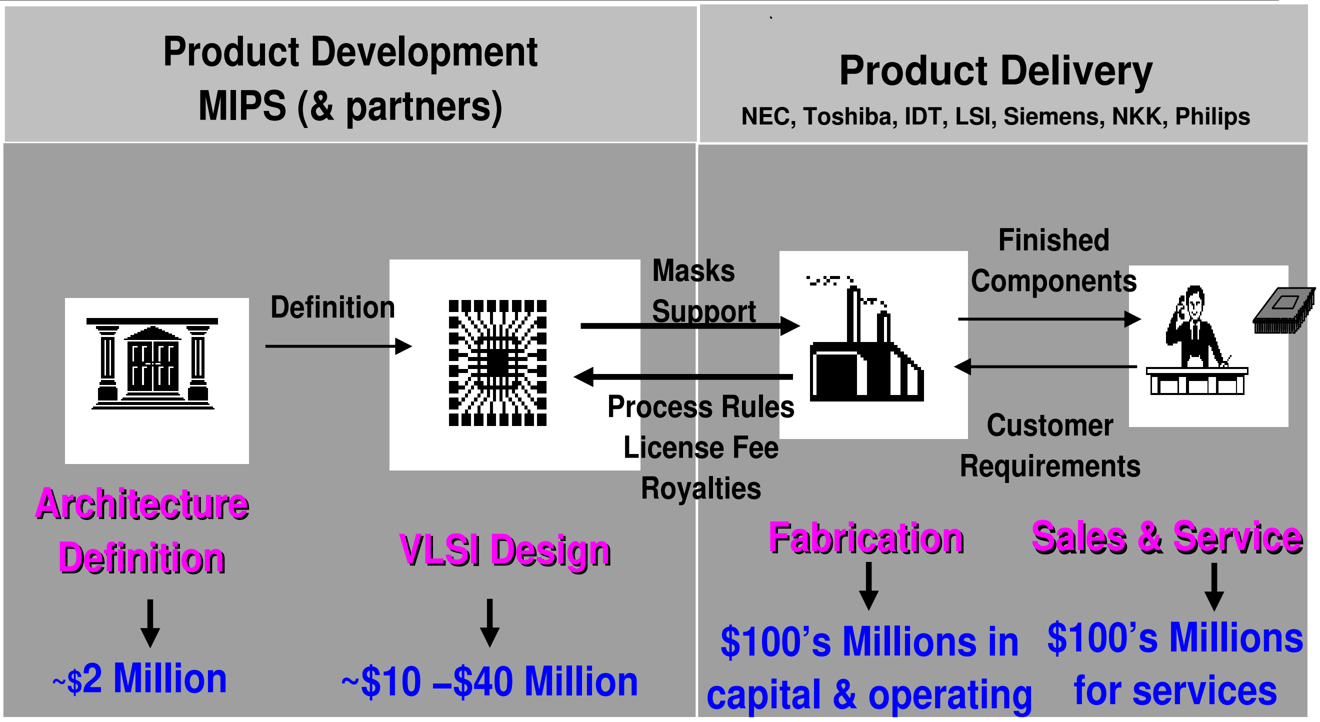

La gente dice que cuesta 1 Billón $ desarrollar un nuevo chip. Ni hablar !!!
La fábrica (de chips) puede costar eso. El coste de diseño mucho menos.

R10000: Especificaciones de diseño

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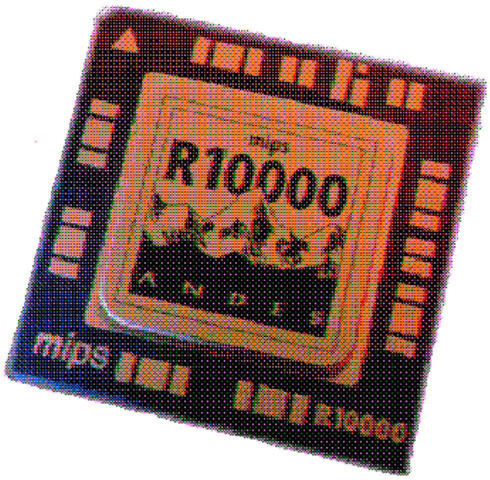
- Propósito general, altas prestac.
- reducir sensibilidad a la secuencia de código (ordenación instruc.) y a la latencia de memoria
- múltiples suministradores (fabricantes)
- CMOS 0.35micras
- un solo chip



Características Técnicas

– 4 way superescalar

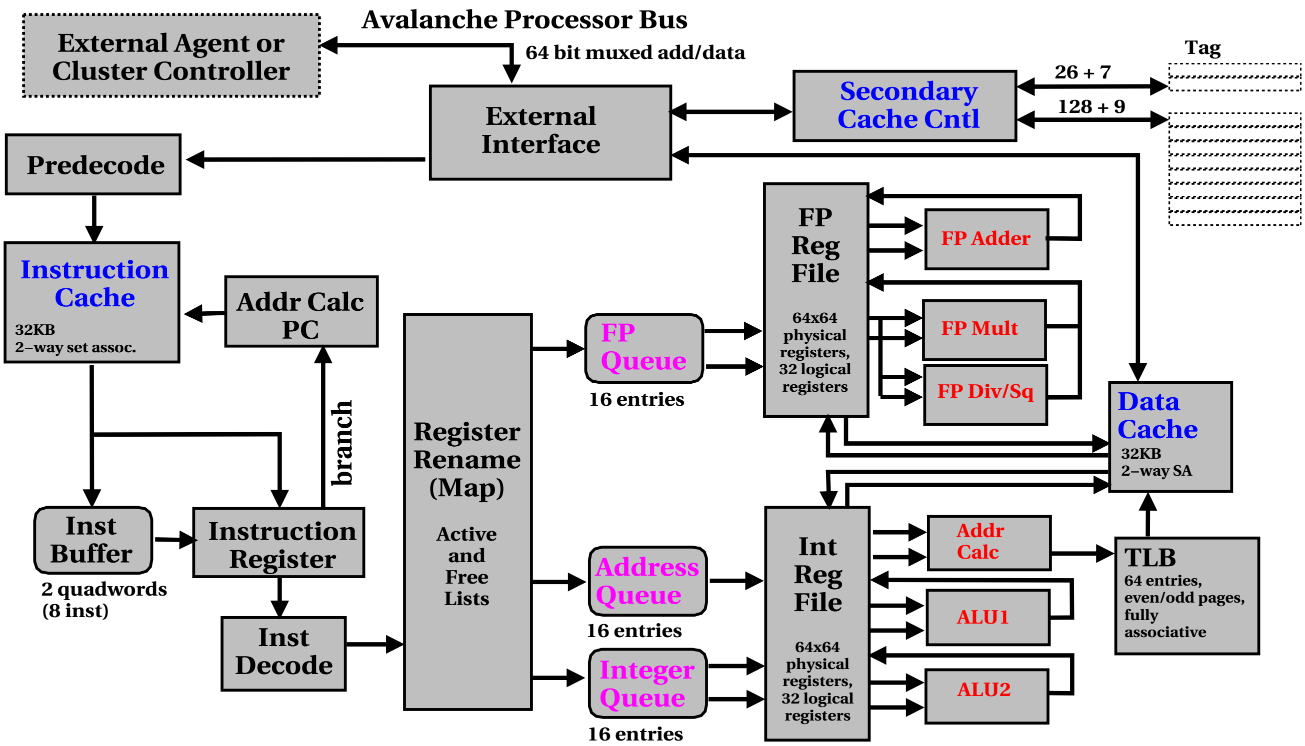
– ANDES architecture:
Architecture with Non–sequential
Dynamic Execution Scheduling

– 64 bit

– 11 SPECint95 – 19 SPECfp95 @ 200MHz

– Diseño específico para Origin

Diagrama de bloques R10000



Layaout R10000

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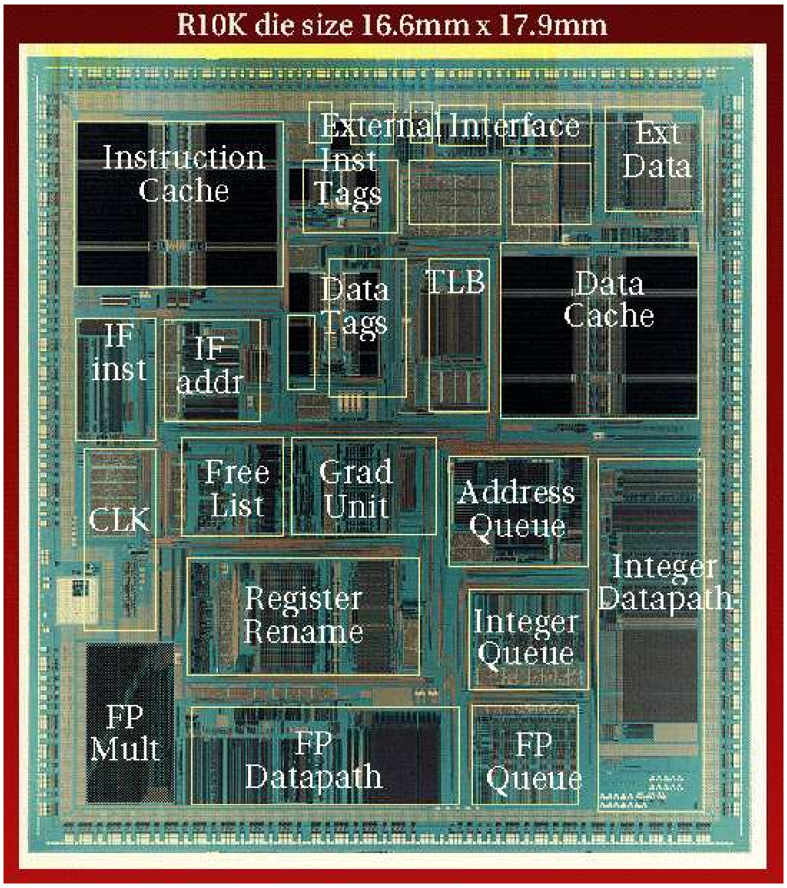

Detalles del R10000

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Pipeline Freq.	**200 MHz**
Power/Voltage	**30 Watts/3.3 V @ 200 MHz**
On–chip cache	**32 KB inst, 32 KB data, both 2–way**
Ext. sec cache	**up to 16MB, 2–way, synch SRAM**
Process	**CMOS: 0.5m drawn, 0.35m Leff, 4 Layers**
Die Size	**16.8 x 18.1 mm, 304 mm2**
Transistors	**5.2 (caches: 3.6 M, logic: 1.6 M)**
Packages	**599–pin plastic LGA, electrically–enhanced**
Initial Suppliers	**NEC, Toshiba**

Problemas/Soluciones

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Latencia de memoria

- non–blocking cache –>
- prefetch
- dedicated cache bus

Dependencia de datos

- out of order execution –>> register renaming

Branches

- branch prediction –>>> speculative execution

non–blocking cache

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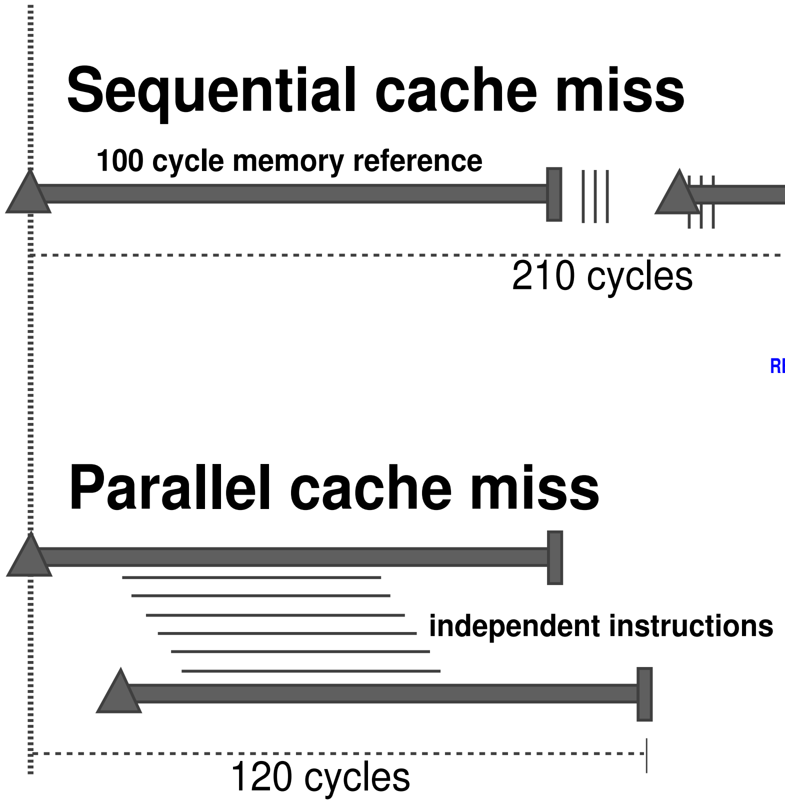

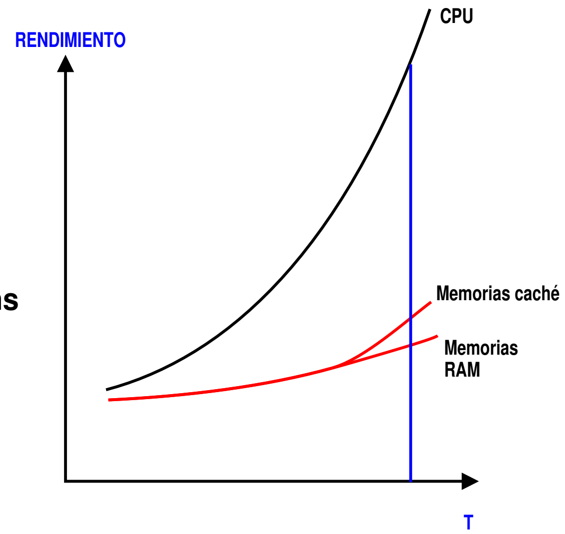

Out–of–order execution

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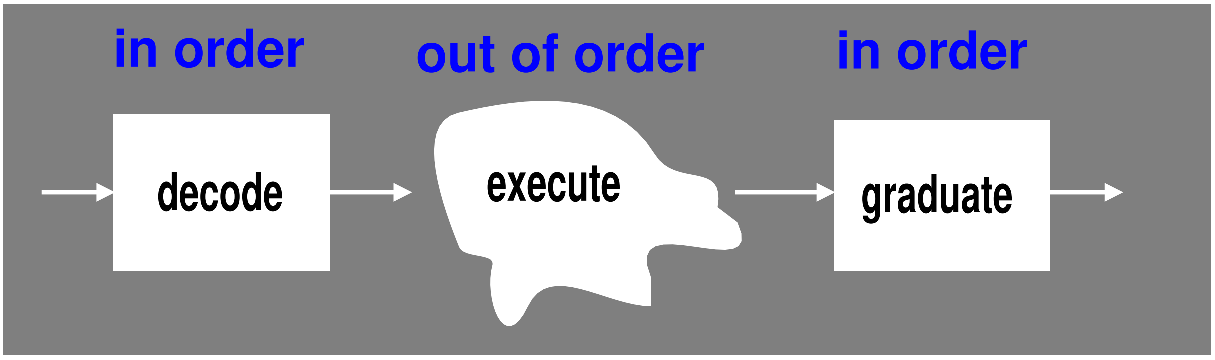

Register renaming

Virtualizes register resources at instruction level

latency tolerance
branch speculation
precise exceptions

Out–of–order execution

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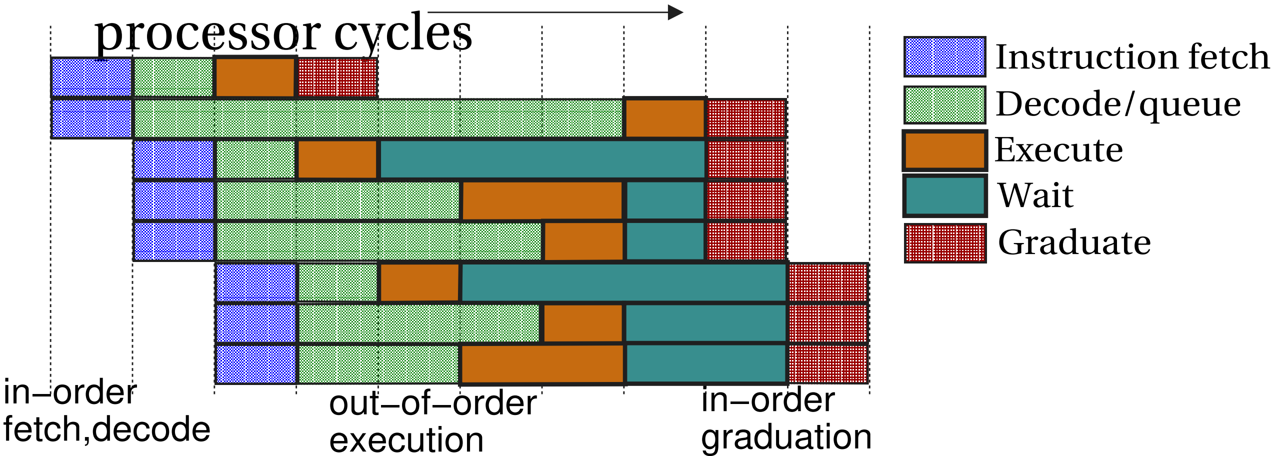

- Up to 32 instructions on the "active list" at a time
- Instructions issued when operands ready and unit is available
- Register renaming used to resolve dependencies
  - –each new instr's logical dest reg mapped to a free physical reg
  - –up to 63 registers available on "free list", 65 are committed state
  - –R10000 contains 64 physical int registers, 64 physical FP registers (all 64–bit)

branch prediction

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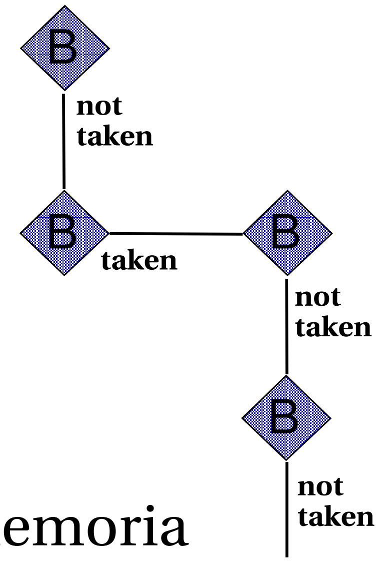

- Especulates en las "branches"
- Hasta 4 niveles de branch predictions
- hast 32 instrucciones en marcha
- Un solo ciclo para cancelar branches

➡ Previene interferencies de memoria

➡ Anticipa fallos de memoria y ejecuta prefetch

R10000 DATA FLOW

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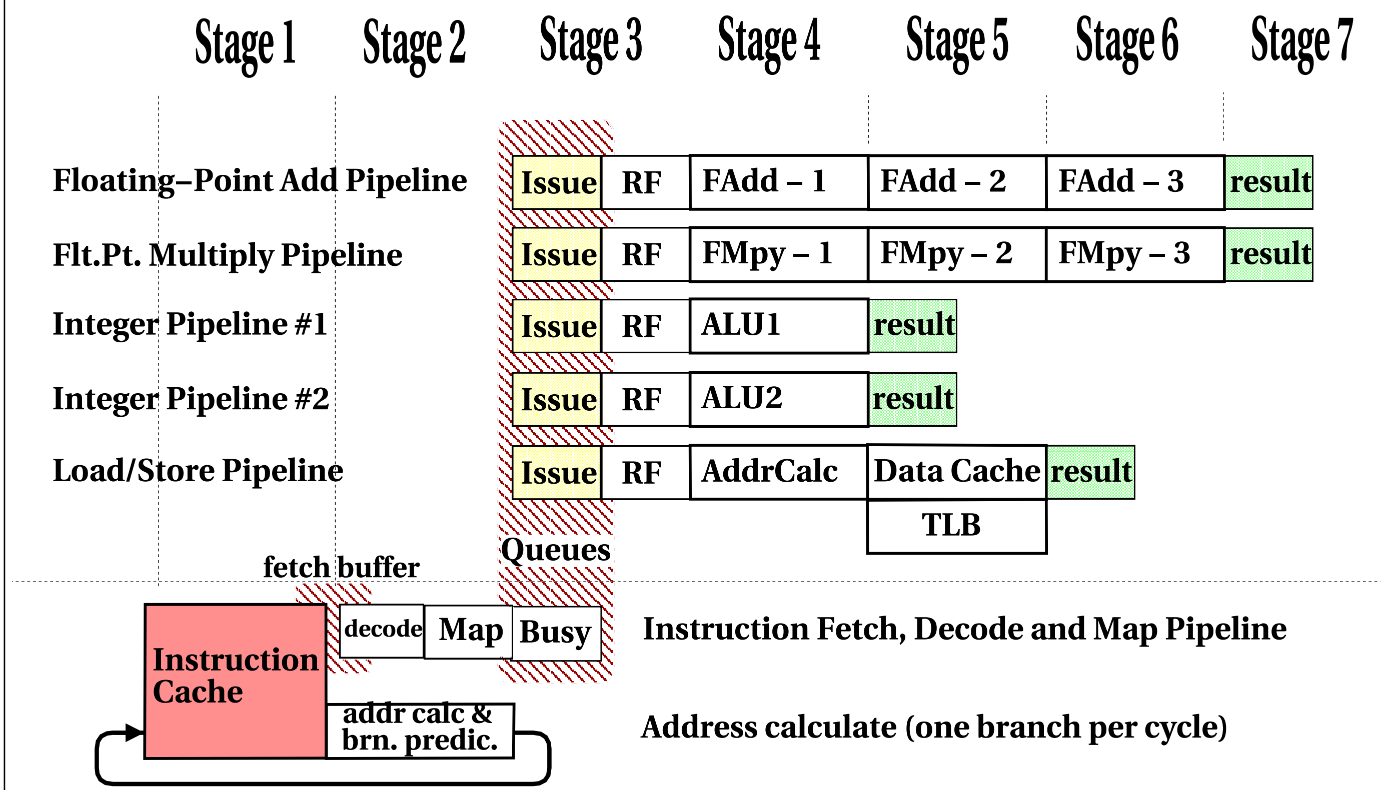

Latencia de las instrucciones

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INTEGER	***Latency***	***Repeat Rate***
ALU1		
add, sub, logic ops, shift, branches	1	1
ALU2		
add, sub, logic ops	1	1
multiply (32–bit, signed, LO/HI)	5/6	6
multiply (64–bit, signed, LO/HI)	9/10	10
divide (32–bit/64–bit)	35/67	35/67
LOAD/STORE		
load (primary cache–hit. int/FP)	2/3	1
store (dirty hit in primary)	–	1
FLOATING POINT		
add, compare, convert	2	1
multiply	2	1
multiply–add, MADD (bypass/not)	2/4	1
divide (single/double)	9/17	8/16
sqrt (single/double)	16/30	15/29

Avalanche™ Processor Bus

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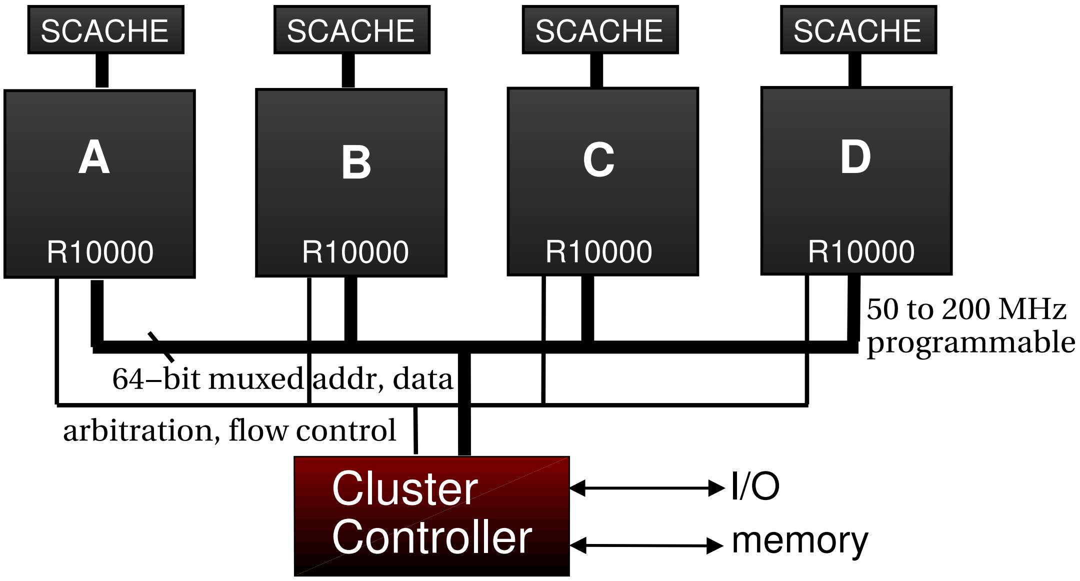
- direct–connect 2 to 4–way multiprocessing
- programmable bus speed (up to 1.5 GB/sec peak refill)
- uncached accelerated writes, incoming/outgoing buffers
- up to 8 outstanding split transactions (4 per processor)
- supports snoopy and directory–based coherency
- HSTL (low voltage swing) or CMOS/TTL levels



R10000 Caches

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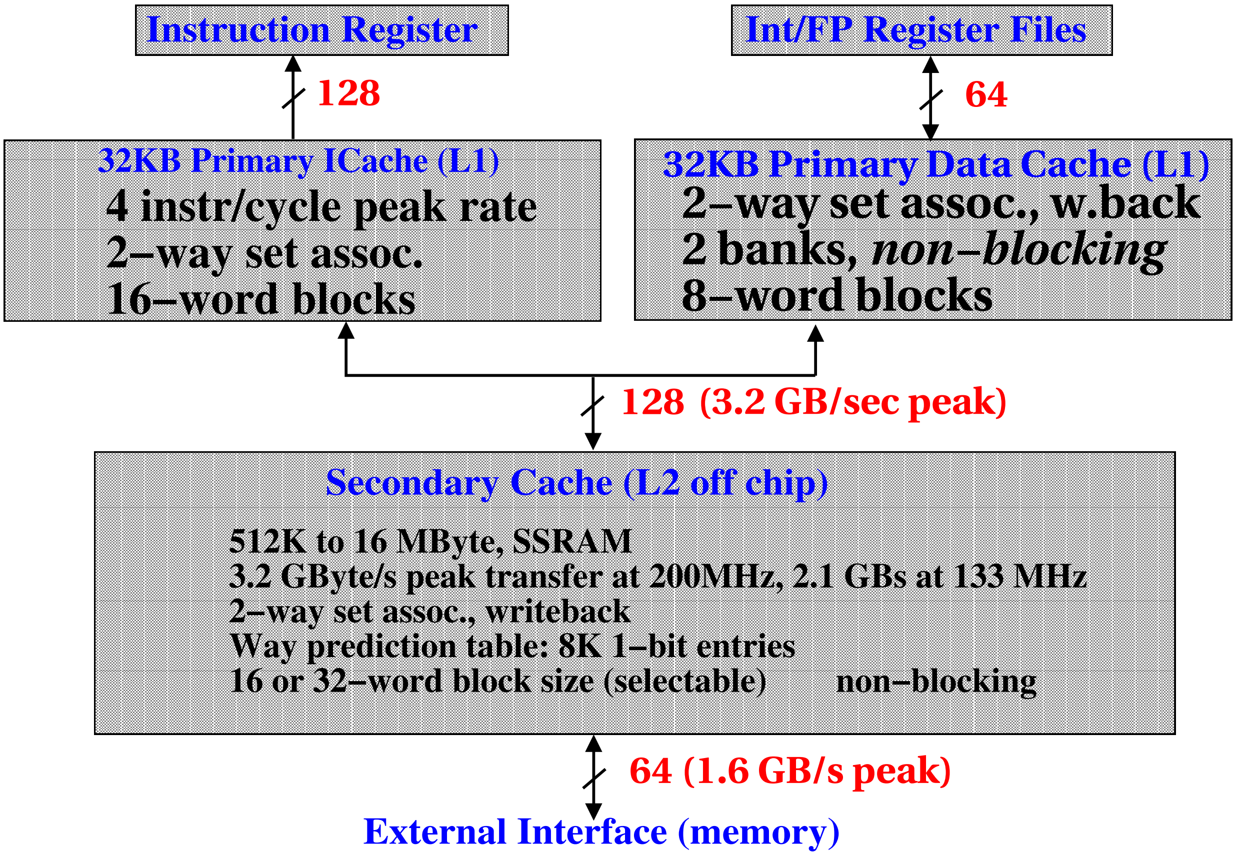

Performance Counters

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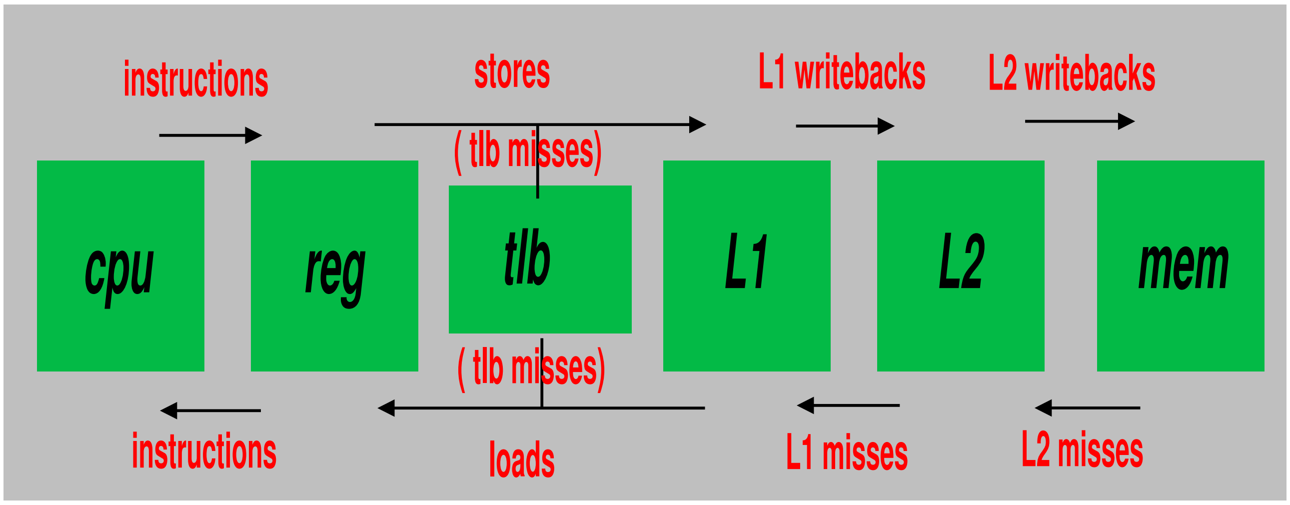
Para estudiar el comportamiento del procesador y del acceso a memoria



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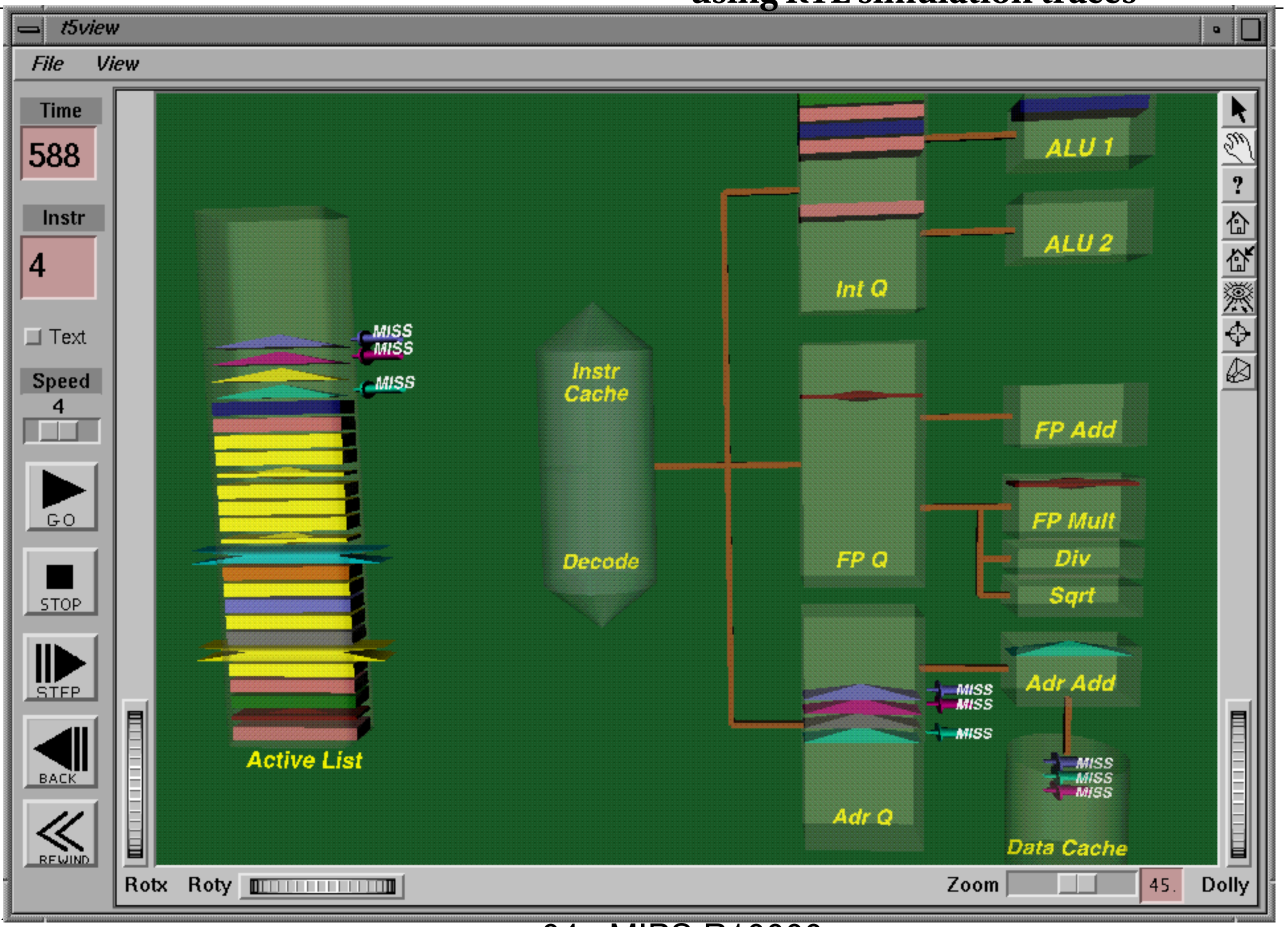
R10000 visual model

Inventor–based visual pipeline demonstration using RTL simulation traces



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Tipos de códigos